Fig.1

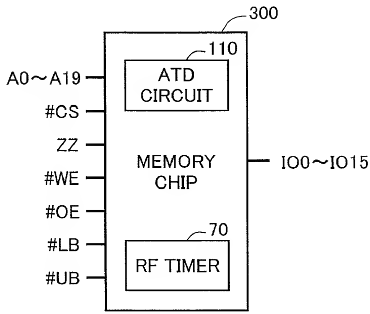


Fig.2

	#CS	ZZ	REFRESH MODE (Note)
OPERATION	L	H	MODE 1
STANDBY	H	H	MODE 1
SNOOZE (POWER DOWN)	H	L	MODE 2

(Note)

Refresh mode 1: refresh operation performed in sync with ATD signal after refresh timing signal issued in memory chip

Refresh mode 2: refresh operation performed in response to generation of refresh timing signal in memory chip (address input not required)

SUMMARY OF OPERATION

Fig.3(a) ATD
Fig.3(b) #CS
Fig.3(c) ZZ
Fig.3(d) A0~A19
Fig.3(e) #WE
Fig.3(f) #OE
#LB,#UB
Fig.3(g) DATA
Fig.3(h) CYCLE

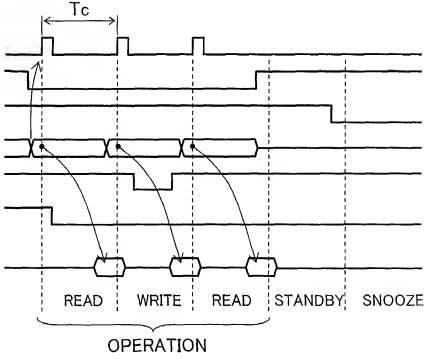


Fig.4

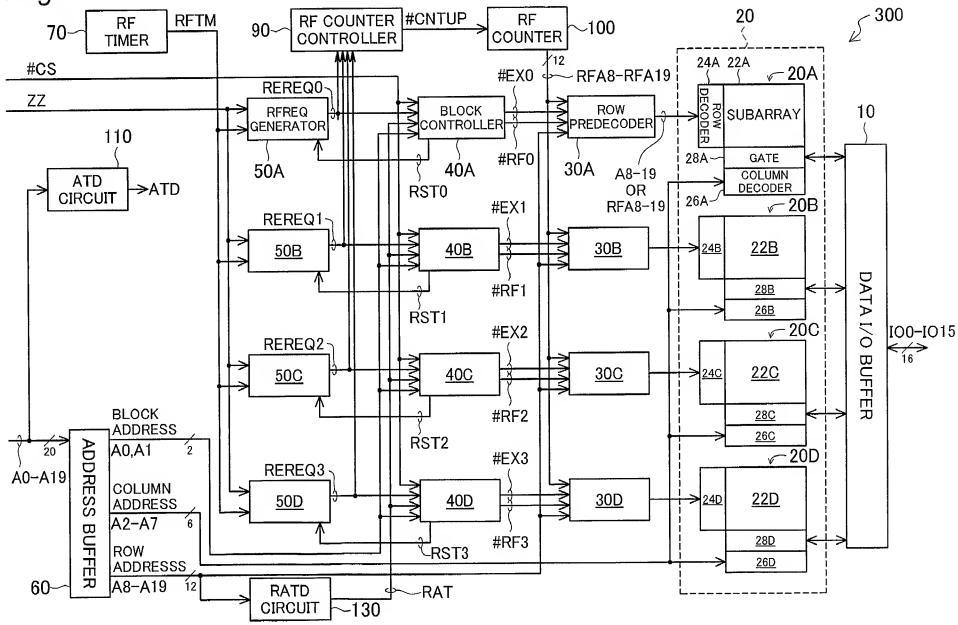

70
RF TIMER
RFTM
90
RF COUNTER CONTROLLER
#CNTUP
RF COUNTER
100
20
300
#CS
ZZ
REREQ0
RFREQ GENERATOR
50A
BLOCK CONTROLLER
40A
#EX0
#RF0
RST0
12
RFA8-RFA19
ROW PREDECODER
30A
A8-19 OR RFA8-19
24A
22A
20A
ROW DECODER
SUBARRAY
10
28A
GATE
COLUMN DECODER
26A
110
ATD CIRCUIT
ATD
REREQ1
50B
40B
#EX1
#RF1
RST1
30B
20B
24B
22B
28B
26B
REREQ2
50C
40C
#EX2
#RF2
RST2
30C
20C
24C
22C
28C
26C
IO0-IO15
16
DATA I/O BUFFER
REREQ3
50D
40D
#EX3
#RF3
RST3
30D
20D
24D
22D
28D
26D
BLOCK ADDRESS
A0,A1
2
20
A0-A19
ADDRESS BUFFER
COLUMN ADDRESS
A2-A7
6
ROW ADDRESSS
A8-A19
12
60
RATD CIRCUIT
130
RAT

Fig.5

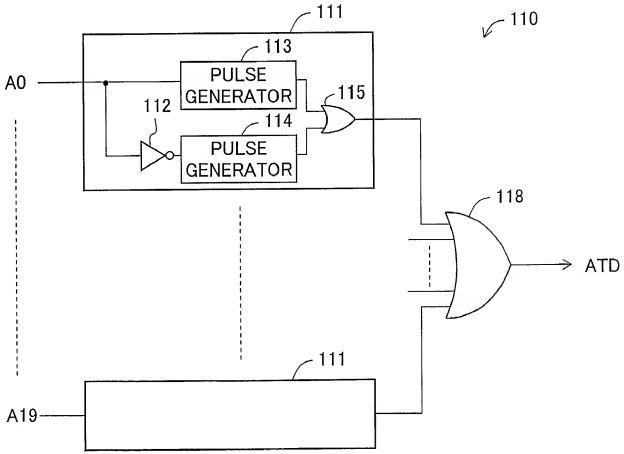

111
110
113
A0
PULSE GENERATOR
115
112
114
PULSE GENERATOR
118
ATD
111
A19

Fig.6

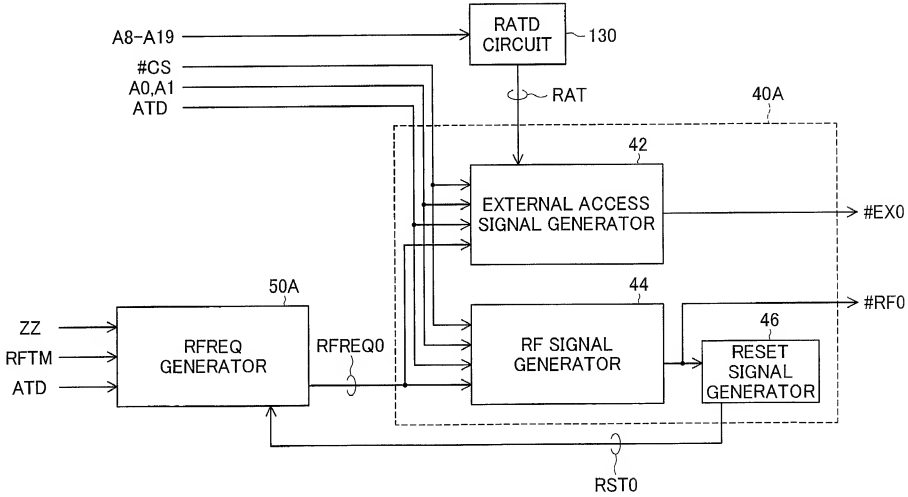


Fig.7

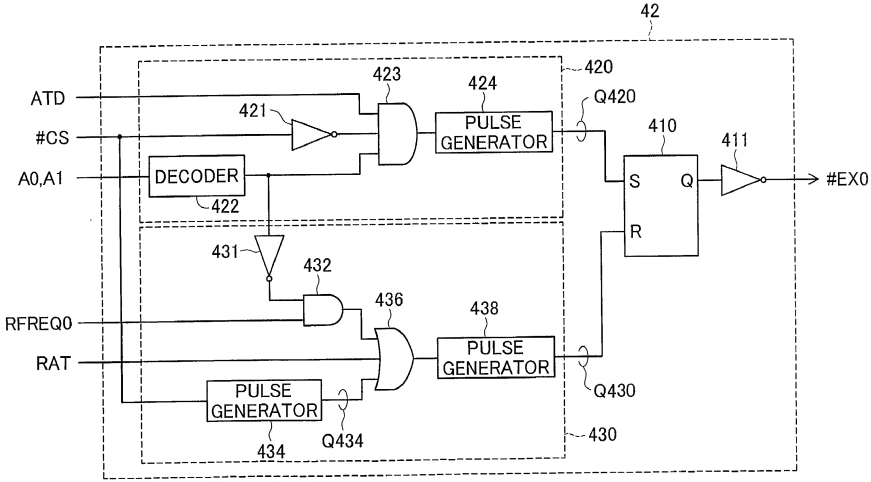
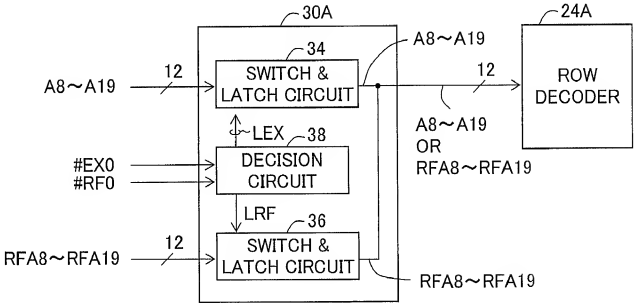
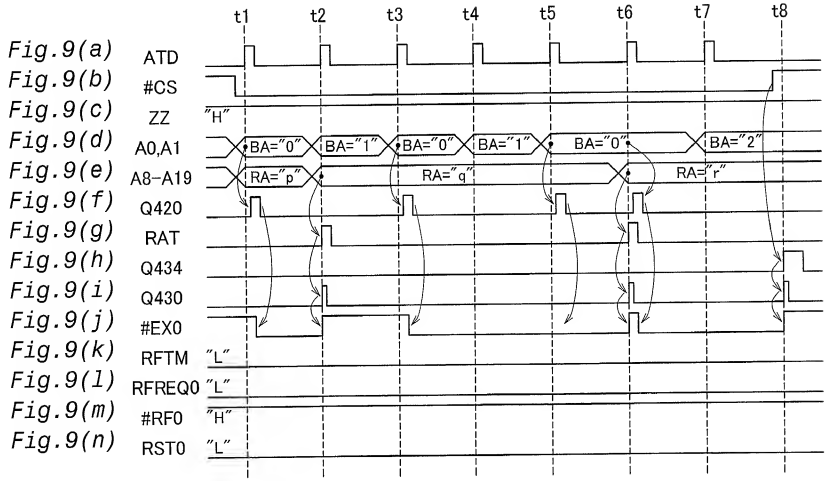
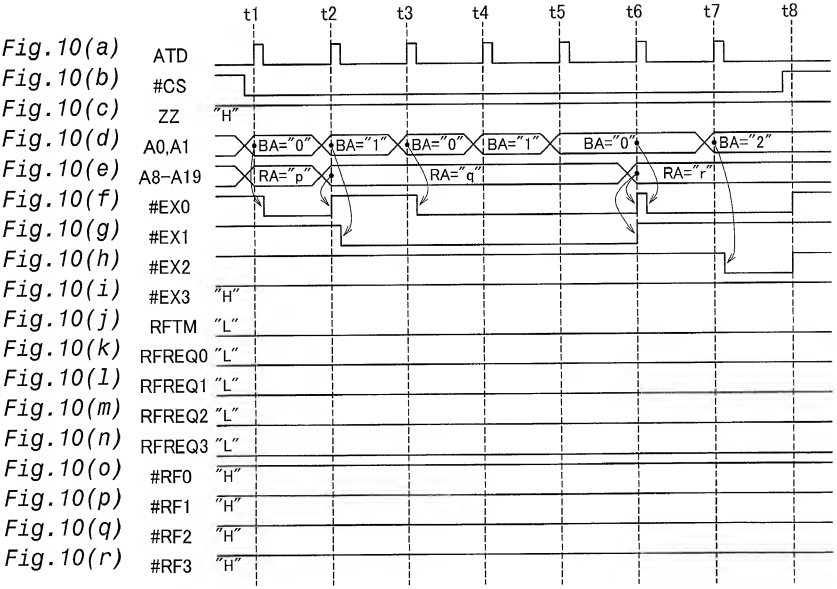

42
420
423
424
ATD
421
PULSE GENERATOR
Q420
410
411
#CS
S
Q
#EX0
A0,A1
DECODER
422
R
431
432
436
438
RFREQ0
RAT
PULSE GENERATOR
Q430
PULSE GENERATOR
Q434
434
430

Fig.8




t1
t2
t3
t4
t5
t6
t7
t8
Fig.9(a) ATD
Fig.9(b) #CS
Fig.9(c) ZZ
"H"
Fig.9(d) A0,A1
BA="0"
BA="1"
BA="0"
BA="1"
BA="0"
BA="2"
Fig.9(e) A8–A19
RA="p"
RA="q"
RA="r"
Fig.9(f) Q420
Fig.9(g) RAT
Fig.9(h) Q434
Fig.9(i) Q430
Fig.9(j) #EX0
Fig.9(k) RFTM
"L"
Fig.9(l) RFREQ0
"L"
Fig.9(m) #RF0
"H"
Fig.9(n) RST0
"L"


t1
t2
t3
t4
t5
t6
t7
t8
Fig.10(a) ATD
Fig.10(b) #CS
Fig.10(c) ZZ "H"
Fig.10(d) A0,A1 BA="0" BA="1" BA="0" BA="1" BA="0" BA="2"
Fig.10(e) A8-A19 RA="p" RA="q" RA="r"
Fig.10(f) #EX0
Fig.10(g) #EX1
Fig.10(h) #EX2
Fig.10(i) #EX3 "H"
Fig.10(j) RFTM "L"
Fig.10(k) RFREQ0 "L"
Fig.10(l) RFREQ1 "L"
Fig.10(m) RFREQ2 "L"
Fig.10(n) RFREQ3 "L"
Fig.10(o) #RF0 "H"
Fig.10(p) #RF1 "H"
Fig.10(q) #RF2 "H"
Fig.10(r) #RF3 "H"

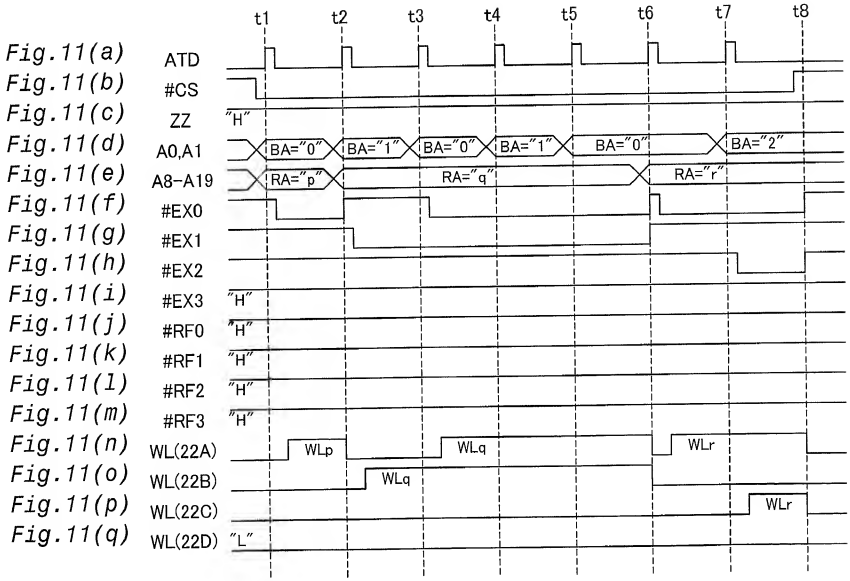
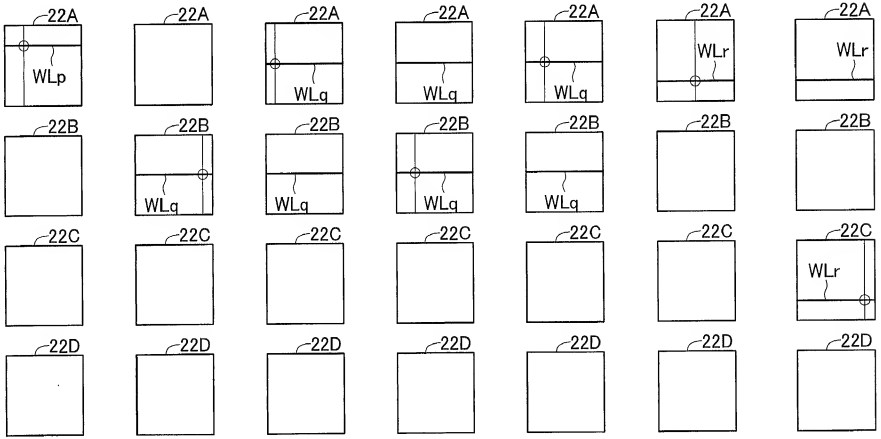
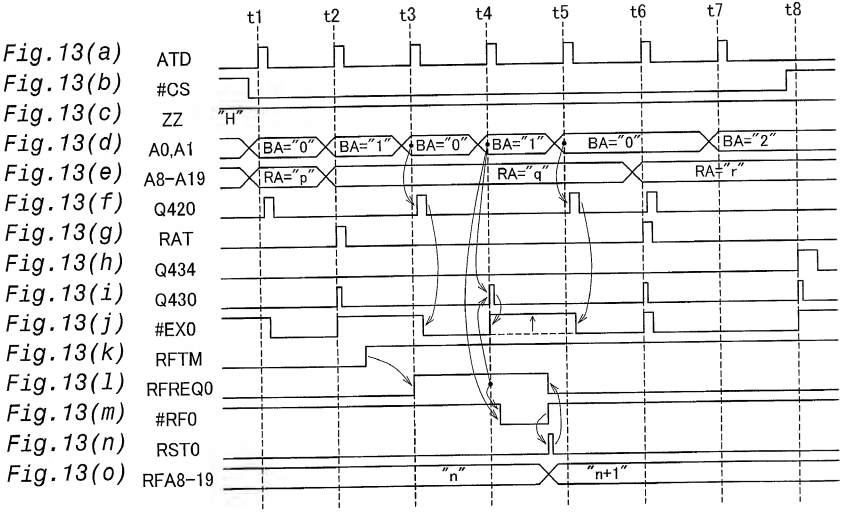

t1
t2
t3
t4
t5
t6
t7
t8
Fig.11(a) ATD
Fig.11(b) #CS
Fig.11(c) ZZ
"H"
Fig.11(d) A0,A1
BA="0"
BA="1"
BA="0"
BA="1"
BA="0"
BA="2"
Fig.11(e) A8-A19
RA="p"
RA="q"
RA="r"
Fig.11(f) #EX0
Fig.11(g) #EX1
Fig.11(h) #EX2
Fig.11(i) #EX3
"H"
Fig.11(j) #RF0
"H"
Fig.11(k) #RF1
"H"
Fig.11(l) #RF2
"H"
Fig.11(m) #RF3
"H"
Fig.11(n) WL(22A)
WLp
WLq
WLr
Fig.11(o) WL(22B)
WLq
Fig.11(p) WL(22C)
WLr
Fig.11(q) WL(22D)
"L"

Fig.12(A) Fig.12(B) Fig.12(C) Fig.12(D) Fig.12(E) Fig.12(F) Fig.12(G)




t1
t2
t3
t4
t5
t6
t7
t8
Fig.13(a) ATD
Fig.13(b) #CS
Fig.13(c) ZZ
"H"
Fig.13(d) A0,A1
BA="0"
BA="1"
BA="0"
BA="1"
BA="0"
BA="2"
Fig.13(e) A8-A19
RA="p"
RA="q"
RA="r"
Fig.13(f) Q420
Fig.13(g) RAT
Fig.13(h) Q434
Fig.13(i) Q430
Fig.13(j) #EX0
Fig.13(k) RFTM
Fig.13(l) RFREQ0
Fig.13(m) #RF0
Fig.13(n) RST0
Fig.13(o) RFA8-19
"n"
"n+1"

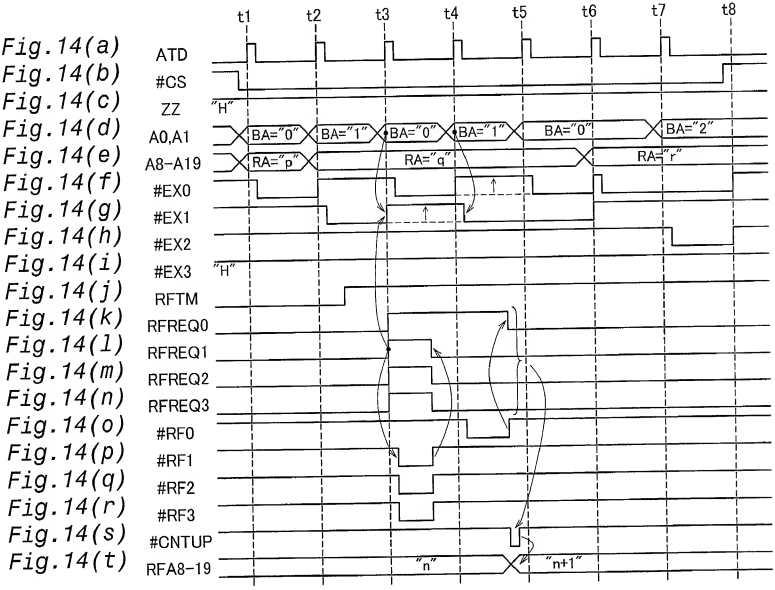
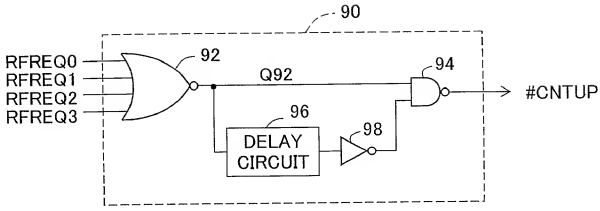


Fig.14(a)
Fig.14(b)
Fig.14(c)
Fig.14(d)
Fig.14(e)
Fig.14(f)
Fig.14(g)
Fig.14(h)
Fig.14(i)
Fig.14(j)
Fig.14(k)
Fig.14(l)
Fig.14(m)
Fig.14(n)
Fig.14(o)
Fig.14(p)
Fig.14(q)
Fig.14(r)
Fig.14(s)
Fig.14(t)

Fig.15



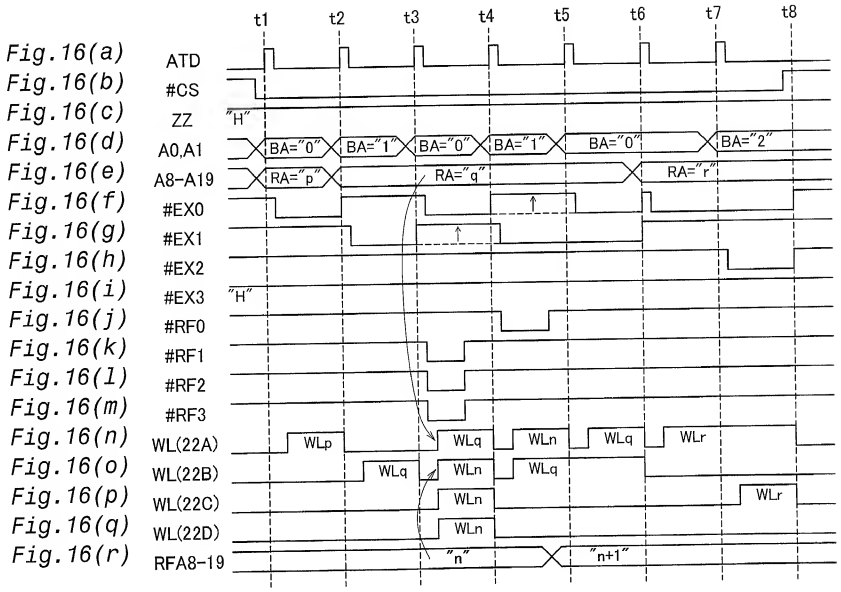
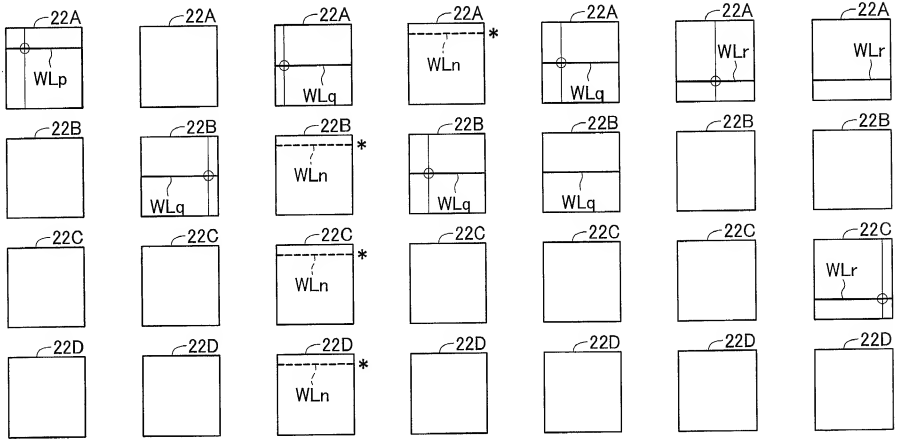
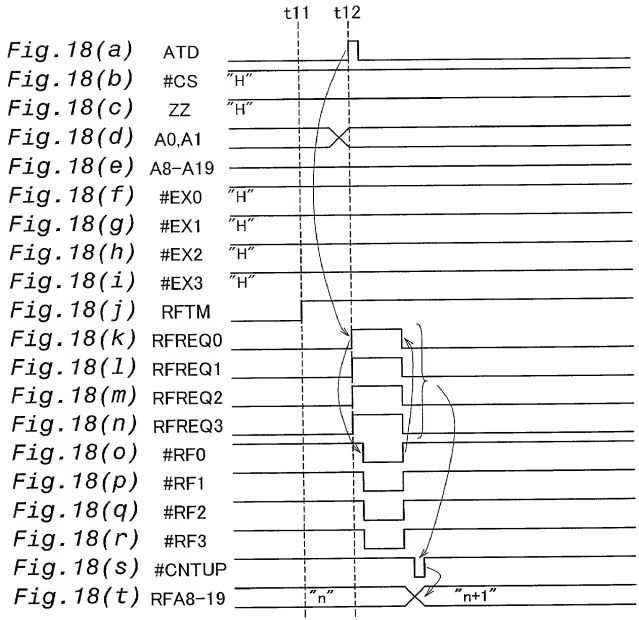


Fig.16(a)
Fig.16(b)
Fig.16(c)
Fig.16(d)
Fig.16(e)
Fig.16(f)
Fig.16(g)
Fig.16(h)
Fig.16(i)
Fig.16(j)
Fig.16(k)
Fig.16(l)
Fig.16(m)
Fig.16(n)
Fig.16(o)
Fig.16(p)
Fig.16(q)
Fig.16(r)

Fig.17(A) Fig.17(B) Fig.17(C) Fig.17(D) Fig.17(E) Fig.17(F) Fig.17(G)





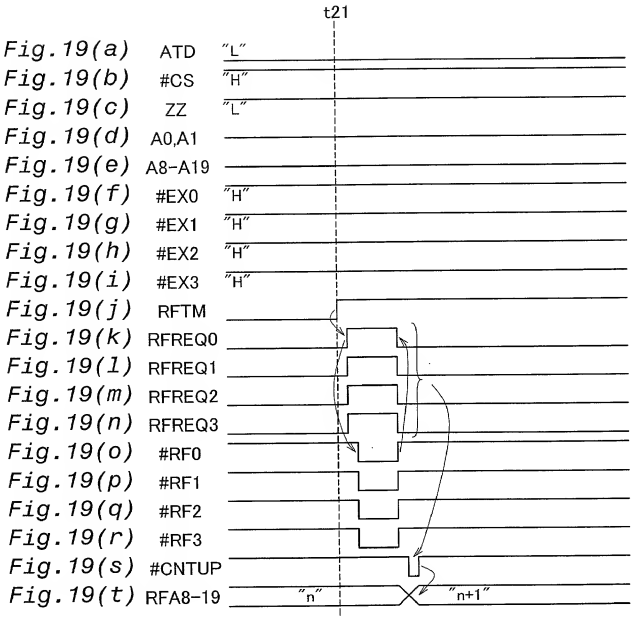


Fig.20

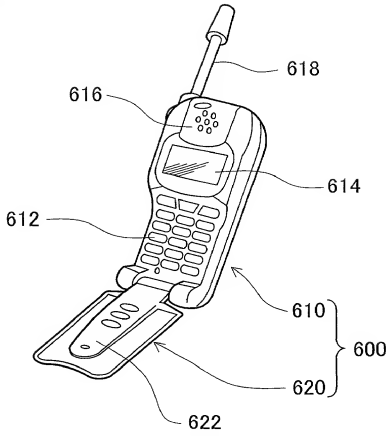
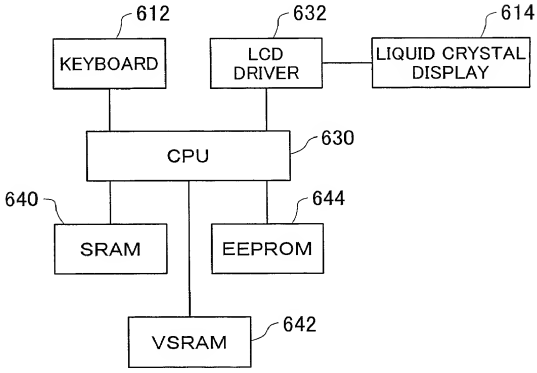

618
616
614
612
610
600
620
622

Fig.21


612
632
614
KEYBOARD
LCD DRIVER
LIQUID CRYSTAL DISPLAY
CPU
630
640
644
SRAM
EEPROM
VSRAM
642